A 6-bit, 0.1-V DAC Based on an M-2M Ladder Network in IBM 130 nm CMOS

A. Kvitschal[1 2], C. C. Santos Jr.[1], L. K. Slongo[1], R. M. da Ponte[1] and C. Galup-Montoro[1]
[1]Department of Electrical Engineering, UFSC, Florianópolis, SC, Brazil
[2]Chipus Microelectronics, Florianópolis, SC, Brazil

***Abstract*—This paper presents the design of an ultralow-voltage DAC using a transistor-only R-2R ladder network in the IBM 130 nm CMOS technology. The building blocks of the converter are firstly described, which include a binary current division circuit and an amplifier both operating in the subthreshold region. Then the whole DAC performance is evaluated through system simulations. The converter is intended to operate from a supply voltage of 0.1 V, showing a dynamic power consumption of 41.1 nW and a maximum operating frequency of 20 kS/s while maintaining an INL below 1 LSB.**

I. Introduction

As the demand for low-power and low-voltage devices increases, it is essential to design microelectronics circuits that are able to operate at very low-voltage supplies, consuming as least power as possible in order to reduce the costs.

Analog-to-digital (ADC) and digital-to-analog (DAC) converters are ubiquitous components in analog and mixed-signal circuits, playing a crucial role in electronics systems, as they provide the interface between the silicon chip and the real world. An important characteristic of data converters is the current or voltage division required to perform the quantization technique. In DACs the analog output is obtained through some scaling circuitry using a voltage or current reference [1].

The most commonly used binary current division circuit is the R-2R ladder network, which can realize a very linear current division technique at the expense of silicon area. M-2M ladder networks are the MOSFET-based version of resistor R-2R networks and do not consume too much silicon area, being quite suited for low-power and low-voltage applications [2].

In this paper, we report some simulation results of a 6-bit DAC powered by an ultralow-voltage supply of 0.1 V using the IBM 130 nm CMOS technology. The whole converter is designed to operate in the weak-inversion region and uses an M-2M ladder network as the binary division circuitry and an amplifier to implement the current-to-voltage conversion. The DAC specifications include an INL (Integral Nonlinearity) of 1 LSB (Least Significant Bit) and a maximum operating frequency of 20 kS/s. The circuit shows a maximum dynamic power consumption of 41.1 nW. To the best knowledge of the authors, this is the first attempt to design a digital-to-analog converter at such a low-voltage supply.

Firstly, section II presents the system-level requirements of the DAC. In section III, the M-2M ladder network is explained and section IV describes the amplifier. Then section V shows the performance of the whole DAC.

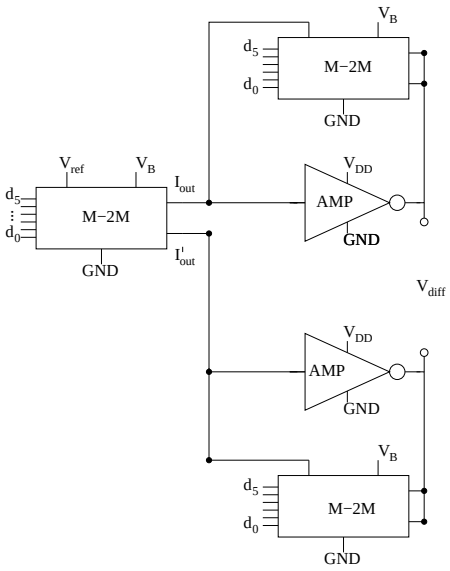

Fig. 1. System-level architecture of the DAC.

II. The Digital-to-Analog Converter

The architecture of the DAC is shown in figure 1. The converter uses the output currents I_{out} and $I'_{out}$of the M-2M network and two amplifiers with negative feedback to generate a differential output proportinal to the digital word D applied to the network control pins d_0 to d_5.

Both amplifiers used in the circuit are configured as I-V converters. With a resistive feedback load, the output voltage is proportional to the input current plus a biasing voltage. Considering that the same M-2M network can be used as a feedback load, matching between the input network and feedback load is improved and hence the whole circuit is less sensitive to process and temperature variations. Also, substituting resistors for MOSFETs operating in the linear region is less area-consuming.

The use of a differential setup helps compensating non-linearites and the commom-mode voltage needed to bias the amplififer. If the matching of the two amplifiers is guaranteed through layout techniques, the M-2M network mismatch due to voltage offsets between the two output currents is greatly reduced.

When specifying an AD or DA converter, there are some main characteristics to be specified: the number of bits, maximum integral (INL) and differential (DNL) error and other

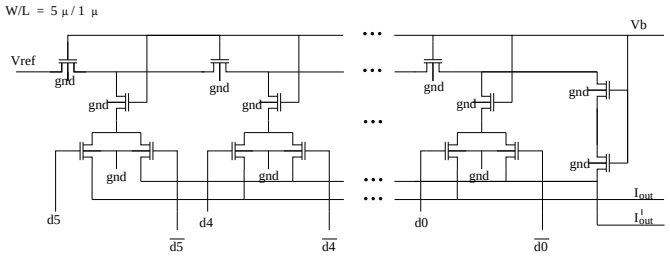

Fig. 2. Simplified schematic of a 6-bit M-2M ladder network operating in subthreshold region and under 0.1 V of voltage reference

functional specifications like voltage and temperature range. The higher the number of bits, higher will be the requirements for the accuracy of the M-2M network and amplifier [3].

Given the extremely low voltage requirements imposed for this work, achieving an amplifier with high gain and sufficient output swing was one of the major concerns. Considering this, it is important to specify the minimum requirements in gain and bandwidth for the amplifier during the system-level analysis.

Errors on the M2M network output current are the result of many different factors. The most significant ones are parameters mismatch, different saturation levels and voltage offset between outputs. The first two of them are controlled by design parameters, but the last one must be guaranteed by the system topology.

Since the system is being pushed to the lowest voltage and the lowest power operation and the amplifier gain is highly affected by biasing current and drain-to-source voltage, it is important to know the minimum gain for this block that will still satisfy the system accuracy requirements.

Considering an amplifier with limited gain, the error introduced by this block can be calculated as a function of the gain. The amplifier output voltage is shown in equation 1.

$$V_o = -I_{out}R_F + \frac{I_{out}R_F}{A+1} \tag{1}$$

where A is the gain, R_F is the feedback resistance and I_{out} is the M-2M ladder output current. The rightmost term in equation 1 refers to the error.

It is important to remark that the error is not constant with the current. It should also be noted that the amplifier introduces a gain error that is maximum at the end of the scale.

Since the error of each block varies along the scale, the final error of the system is smaller than or equal to the sum of all blocks errors.

III. M-2M Ladder Network

In this section, we introduce a 6-bit M-2M ladder network proposed to operate in subthreshold region and under 0.1-V reference potential.

Figure 2 presents a simplified schematic of the ladder network implemented to perform the DAC weighting through sucessive binary divisions of the input current generated at the voltage reference node (V_{ref}), which together with potential V_b defines the inversion level of the transistors. The current divisions are possible because M-2M ladder transistors operate in the linear region. In this case, saturation is not a desirable DC condition and bias must be carefully chosen to provide the best linearity, such that it does not introduce significant distortion.

The two bottom transistors are drain-connected in order to deviate the binary fraction of the input current to the nodes either I_{out} or I'_{out}. That will depend on the state of the logic input data connected to each transistor gate. Nodes I_{out} and I'_{out} are then connected to amplifiers in order to present the desired value of quantized current.

The M-2M ladder design involves transistor sizing under some specified biasing conditions and considering identical all of ladder devices. Care must be taken to minimize mismatch and short-channel effects, such as carrier velocity saturation and channel-length modulation. Therefore our methodology mainly aims to satisfy two key issues:

1) a certain channel length is required to prevent short-channel effects, complying with the desired inversion level to achieve a specific transition frequency;
2) a suitable transistor area (WL) is needed to reduce mismatch, which is characterized by the Pelgrom's Model [4] in this work, although more accurate models had already been shown [5].

Mismatch are time-independent variations between identically designed devices in an integrated circuit due to the spatial fluctuations in the technological parameters and geometries [6]. The Pelgrom's Model is the most widely used for determining sufficient sizing of transistors in order to prevent mismatch. This model is presented by equation 2:

$$\sigma(\Delta V_{T0}) = \sqrt{2}\sigma V_{T0} = \frac{q\sqrt{2x_d N_a}}{C'_{ox}\sqrt{WL}} = \frac{A_{VT}}{\sqrt{WL}}, \tag{2}$$

where ΔV_{T0} is the standard deviation of the difference between the threshold voltages of two identical transistors V_{T1} - V_{T2}, N_a is the substrate doping, C'_{ox} is the oxide capacitance per unit area, x_d is the depletion depth and A_{VT} is the mismatch coefficient of the threshold voltage.

To cope with (1), some simulations were realized to match a desired value of channel length with the subthreshold operation (i_f = 0.6) for a intrinsic transition frequency equals to 1 MHz. Thus, for these conditions, we have used a channel length of 1 μm which also avoids undesirable short-channel effects.

To comply with (2), we have determined a value of mismatch parameter A_{VT} about 2.5 $mV - \mu m$ and depicted a curve of the transistor area as a function of the standard deviation $\sigma(\Delta V_{T0})$, shown in figure 3.

One can observe from figure 3 that an area WL of 6 μm gives a value of $\sigma(\Delta V_{T0})$ approximately equals 1 mV. However, in this work, an area of 5 μm^2 has been used since it gives a negligible value of mismatch and also has provided a good linearity for the DAC operation.

Another important issue to consider for proper circuit operation is the sampling related to the degradation of the

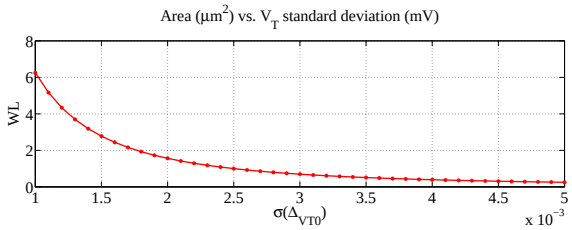

Fig. 3. Transistor area WL as a function of the standard deviation based on Pelgrom's Model.

ratio of "on" conductance to "off" current. Some possible circuit implementations to reduce this effect are related in [7]. However, simulations have shown satisfactory values of "on" g_{ds} (329.4 nA/V to 570.4 nA/V) and "off" I_{DS} (10.66 nA to 15 nA) for the topology adopted in this work.

IV. Inverter Amplifier

The first step on amplifier design was the MOSFET DC analysis, since transistors are supposed to operate in saturation to achieve a better gain. Since the circuit is powered by 0.1 V, it is of paramount importance to understand in which region it operates. Equation 3 is based on the ACM (Advanced Compact MOSFET) model [8] and determines the drain-to-source saturation voltage in terms of the inversion level.

$$V_{DSsat} = \phi_t \left[\ln\left(\frac{1}{\xi}\right) + (1-\xi)\left(\sqrt{(1+i_f)} - 1\right) \right] \qquad (3)$$

ξ is an arbitrary number much smaller than unity and establishes the ratio between the normalized inversion charge at the drain and source ends. Considering $\xi = 0.01$, the drain-to-source saturation voltage is nearly $4.5\phi_t = 117\ mV$ in weak inversion, which means that the amplifier will inevitably operate in the triode region [9]. This result interferes in the amplifier topology selection, because there are headroom constraints imposed by the low supply voltage, which must be divided to the stacked transistors in series. Some simulations were carried out for the classical operational amplifier topology shown in figure 4. However, the circuit did not show a voltage gain higher than 25 V/V even in the presence of a third amplifying stage.

In addition to standard transistors, the IBM 130 nm CMOS technology allows two other types of transistors: low-V_T and zero-V_T. The type of transistors was also changed, but no improvement was verified, since they present a lower output resistance than that of the standard transistors.

The M-2M V_{ref} was also kept in 0.1 V. This resulted in a low current coming out of the M-2M network. This current, converted to a voltage through the feedback resistance, is not enough to saturate completely the amplifier transistors. Therefore, this work uses cascaded inverters to build up an amplifier, as shown in figure 5. This solution is more suitable than the classical operational amplifier and benefits from the dual effect of the PMOS and NMOS transistors, which simultaneously contribute to the amplifier gain. Simulations were carried out

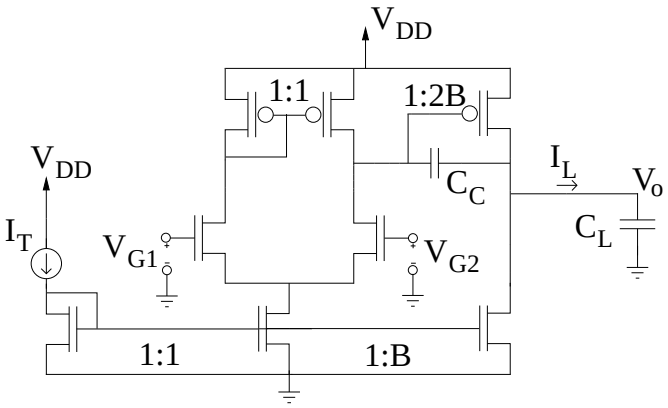

Fig. 4. Classical topology for a two-stage operational amplifier.

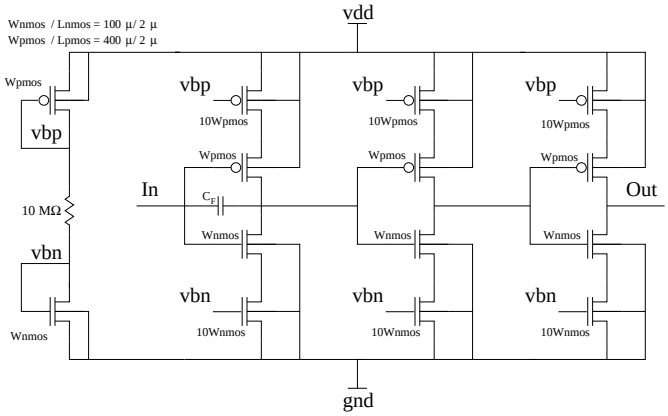

Fig. 5. Amplifier circuit based on cascaded CMOS inverters.

and a topology with three stages of amplification was selected in order to achieve the required gain.

The first simulations for this topology has shown an oscillating behavior. In order to avoid instability, a 1-pF feedback capacitor was placed in the first stage. This has increased the amplifier's phase margin, preventing it from oscillating. The bandwidth decreased by using the capacitor, but it still satisfies the bandwidth requirements ($>$ 20 kHz). The gain curve is shown in figure 6, which indicates a 50-kHz bandwidth for the amplifier and an open-loop gain of nearly 102 V/V. This value is higher than the required gain to make the DA converter work properly. Standard transistors were also used in this topology since they presented better results than those of low-V_T and zero-V_T transistors.

Another issue associated with this topology is the current consumption. The transistors aspect ratio was selected aiming to achieve a gain close to 100 V/V for 0.1 V of voltage supply. When the V_{DD} voltage is increased, the output current tends to augment significantly. Therefore, current mirrors were used to avoid this. When the mirror saturates, all the current flowing through each branche is limited to the current flowing through the 10-$M\Omega$ resistor. Consequently, the amplifier may operate properly with supply voltages higher than 0.1 V.

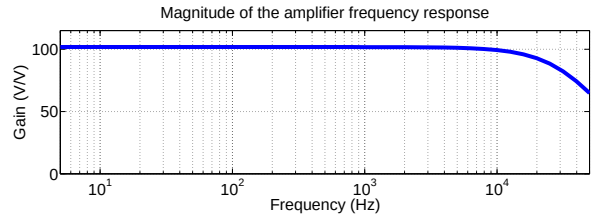

Fig. 6. Magnitude of the amplifier's frequency response.

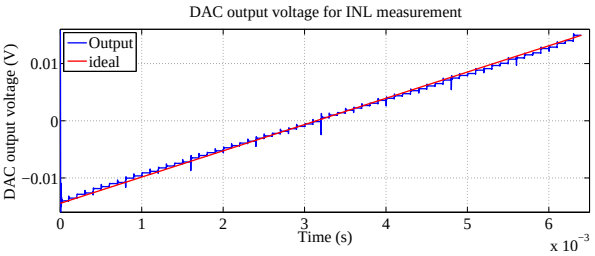

Fig. 7. DAC output voltage and reference straight line to evaluate the INL.

V. Results

In order to analyze the DAC performance, we have evaluated the INL. This is defined as the difference between the converter output voltage and a reference straight line drawn through the first and last output values. These results can be seen in figure 7, which was obtained for an operating frequency of 20 kS/s. The maximum INL was about 800 μV, which is below 1 LSB. In fact this result is nearly equals to $\frac{1}{2}LSB$. Similar simulations for operating frequencies of 1 and 10 kS/s presented INL values around 500 μV and 700 μV, respectively, which are also below $\frac{1}{2}LSB$. In table I, we summarize the main DAC results, which satisfy the specifications, and make a comparison with the ADC presented in [7]. The maximum power consumption refers to the dynamic behavior of the converter.

TABLE I
Summary of DAC Performance Results.

Supply Voltage	0.1 V	0.2 V to 0.9 V
Sampling Frequency	100 S/s to 20 kS/s	2 kS/s to 17.5 MS/s
Power Consumption	41.1 nW	1.66 μW
INL	0.512 LSB	+0.72/-0.90 LSB

VI. Conclusion

In this paper, we report the first attempt to design a DAC operating at 0.1 V, showing the usefulness of the M-2M ladder network as the binary current division technique. The converter also includes a tree-stage amplifier based on the CMOS inverter to cope with the challenges imposed by the low supply voltage. Indeed the simulation results show that the converter consumes only 41.1 nW and maintains an INL below 1 LSB at an operating frequency of 20 kS/s, which covers the entire audio frequency band.

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